

REMARKS

The Examiner is thanked for the thorough examination of this application. The Office Action, however, has continued to reject all presented claims 1-2 and 4-30. In response to the Office Action, claim 12 has been amended. Specifically, claim 12 has been amended to replace “said substrate beneath one said second and third dopent region” with “said substrate under and around one said second and third dopent region”. For at least the reasons that are set forth herein, Applicant respectfully requests reconsideration of the rejections.

Double Patenting Rejection

The Office Action rejected claim 23 on the ground of nonstatutory obviousness-type double patenting, over claim 1 of U.S. patent 6,682,993. Applicant is willing to file a terminal disclaimer to overcome this rejection, after receiving a notice of allowable subject matter.

As to the double patenting rejection of claim 24, this rejection is rendered moot by Applicant's cancellation of that claim.

35 U.S.C. 103(a)

Claims 1-30 stand rejected under 35 U.S.C. 103 (a) as allegedly unpatentable over the acknowledged prior art, in view of Chen et al., Patent No. 6,858,900. Applicant respectfully requests reconsideration for at least the following reasons.

Claim 1

Claim 1, recites:

1. A protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said circuit comprising:

at least one switching circuit string composed of a first and second NMOS device and a PMOS device, wherein the gate of said first NMOS device is connected to a first voltage source and the drain element of said first NMOS device is connected to said active devices input/output signal pad and to the drain element of said PMOS device, and the source of said first NMOS device is connected to the drain element of said second NMOS device and the gates of said second NMOS and said PMOS are connected to an internal circuit and the source of said second NMOS is connected to a second voltage source, and the source of said PMOS is connected to a first voltage source; and

a protection discharging means for discharging ESD energy appearing between said first and said second voltage source, wherein said protection discharging means comprising a discharging NMOS device with a first *and a second drain diffusion which extends under and around said first drain diffusion*, the drain of said discharging NMOS device is directly connected to said first voltage source, and the source of said discharging NMOS device is directly connected to said second voltage source.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above. In this regard, neither AAPA nor Chen teach, disclose or suggest a second drain diffusion, which extends *under and around* said first drain diffusion.

In contrast to this claimed teaching, in Chen, p+ pockets 40 can be selectively formed *under any island or any poly gate* within the MOS structure (Col. 5 lines 54-58 and Fig.5) not *under and around* said first drain diffusion and person in the art knows that island 20 (Fig.5 of Chen) is different from the drain diffusion.

For at least this reason, claim 1 is allowable over the cited reference. Insofar as claim 1 is allowable, claims 2 and 4-11, which depend from claim 1, are also allowable on their own merits in claiming additional elements not included in claim 1.

Claim 12

Claim 12, as amended, recites:

12. An effective Vcc to Vss power ESD protection device with reduced junction breakdown voltage connected between Vcc and Vss power bus lines comprising:
a substrate having a first dopent type;
isolation regions within said substrate for isolation of said ESD protection device;
a FET gate with abutting spacers for said ESD protection device;
multiple regions of a second dopent type of opposite dopent to said substrate for said ESD protection device between said gate and said isolation regions;
multiple regions of a third dopent type of opposite dopent to said substrate for said ESD protection device between said gate and said isolation regions;
a special fourth dopent region of similar dopent to said substrate *under and around* one said second and third dopent region;
a protective insulation layer over said ESD protection device; and
first, second and third electrical conductor elements.

(*Emphasis added.*) Claim 12 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above. In this regard, neither AAPA nor Chen teach, disclose or suggest a special fourth dopent region of similar dopent to said substrate *under and around* one said *second and third dopent region*.

In contrast, in Chen, In Chen, p+ pockets 40 can be selectively formed *under any island or any poly gate* within the MOS structure (Col. 5 lines 54-58 and Fig.5) not *under and around* one said *second and third dopent region*, and person in the art knows that island 20 (Fig.5 of Chen) is different from the second and third dopent region.

For at least this reason, claim 12 is allowable over the cited reference. Insofar as claim 12 is allowable, claims 12-22, which depend from claim 12, are also allowable on their own merits in claiming additional elements not included in claim 12.

Claim 23

Claim 23 recites:

23. A method of forming a protection circuit for protecting integrated semiconductor active devices from damage due to ESD voltages appearing on the circuit power bus lines said method comprising:
connecting source region of a used PMOS device and the source and gate of an unused PMOS device to a first voltage source;
connecting the drains of said used and unused PMOS devices to said active devices input/output pad;
connecting the drain of said used PMOS device to a drain of a first used NMOS device, and the drain of said unused PMOS device to a drain of a first unused NMOS device;
connecting the gate of said used PMOS device and the gate of a second used NMOS device to separate logic signal lines;
connecting the gates of said first used and said first unused NMOS devices to said first voltage source;
connecting the source of said first used NMOS device to the drain of said second used NMOS device and connecting the source of said first unused NMOS device to the drain of a second unused NMOS device;
connecting the source of said second used NMOS and the source and gate of said second unused NMOS device to a second voltage source; and
connecting said ESD protection discharging means for discharging ESD energy appearing between and further directly connected to said first and second voltage source, *wherein said ESD protection discharging means comprises a discharging NMOS device with a special diffusion region under and around said device normal drain region.*

(*Emphasis added.*) Claim 23 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above. In this regard, neither AAPA nor Chen teach, disclose or suggest a special diffusion region *under and around* said device normal *drain region*.

In contrast, in Chen, In Chen, p+ pockets 40 can be selectively formed *under any island or any poly gate* within the MOS structure (Col. 5 lines 54-58 and Fig.5) *not under and around* said device normal *drain region*, and person in the art knows that island 20 (Fig.5 of Chen) is different from the drain region.

For at least this reason, claim 23 is allowable over the cited reference. Insofar as claim 23 is allowable, claims 25-30, which depend from claim 23, are also allowable on their own merits in claiming additional elements not included in claim 23.

As a separate and independent basis for the patentability of all claims, Applicant respectfully traverses the rejections as failing to identify a proper basis for combining AAPA with the cited Chen reference. In combining these references, the Office Action stated only that the combination would have been obvious "because p+ pocket implementation have extra function of reducing the breakdown voltage and create junction breakdown much earlier during an ESD event." (Office Action, page 5). This alleged motivation is clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

"The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicant notes that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also

requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a a power ESD protection device, as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some “teaching, suggestion, or reason” to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the “absence of such a suggestion to combine is dispositive in an obviousness determination”).

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be “clear and particular.” Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 (“The absence of such a suggestion to combine is dispositive in an obviousness determination.”).

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000). The rationales relied on by the Office Action in the present application are merely generic statements, that have nothing to do specifically with the structures disclosed in the other references. As such, these rationales cannot be properly viewed as proper motivations for combining the specific teachings of the individual references. Indeed, the generic motivations advanced by the present Office Action could be used to support a combination of ANY references, which is clearly contra to the cited Federal Circuit precedent and the clear intent of 35 U.S.C. § 103.

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

Conclusion

For the reasons as described above, independent claims 1, 12, and 23 are allowable over the cited references. Insofar as all independent claims are allowable, all claims are allowable.

If the Examiner believes that a teleconference would expedite the prosecution of this application, the Examiner is hereby invited to call the undersigned at the address and telephone listed below.

No fee is believed to be due in connection with this amendment and response. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

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